ENGINEERING, INC.

DAQP-12/12H/16 PCMCIA

Data Acquisition System

For Machines with Standard PCMCIA Interface

Users Manual

INTERFACE CARDS FOR PERSONAL COMPUTERS

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Manufacturer's Address:	One Omega Drive P.O. Box 4047 Stamford, CT 06907-0047
Application of Council Directive:	89/336/EEC
Standards to which Conformity is Declared:	* EN50081-1 (EN55022, EN60555-2, EN60555-3) * EN50082-1 (IEC 801-2, IEC 801-3, & IEC 801-4)
Type of Equipment:	Information Technology Equipment
Equipment Class:	Commercial, Residential and Light Industrial
Product Name:	PCMCIA Card
Model Number :	DAQP-12/12H/16

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List of Figures and Tables

1. Introduction

DAQP CARD FEATURES:

- Sampling rate up to 100 kHz with 12 or 16 bit resolution
- 8 differential or 16 single-ended analog input channels, expandable to 256 channels
- Bipolar input range up to ±10 volts
- Software programmable gain selection: 1, 2, 4 or 8 for the DAQP-12/16 and 1, 10, 100 or 1000 for the DAQP-12H
- 2048 sample Data and Scan FIFOs
- 24-bit pacer clock with variable pre-scalers and internal or external clock source
- Digital input/output channels
- Flexible trigger mode (internal/external, one-shot/continuous, rising/falling edge)
- Omega's "DaqSuite" data acquisition software included in addition to drivers for MS-DOS®, Windows 3.xx and Windows 95/98®

The DAQP series card is a PCMCIA type II data acquisition system with 8 differential or 16 single-ended analog input channels. The number of input channels can be expanded to 256 with an input expansion card. DAQP series products include the DAQP-12, the DAQP-16 and the high gain DAQP-12H. The programmable gain settings of the DAQP-12 and DAQP-16 span bipolar input ranges of ±1.25 V (gain = 8), ±2.5 V (gain = 4), ±5 V (gain = 2) and ± 10V (gain = 1), while the DAQP-12H offers a bipolar input range of ±0.01 V (gain = 1000), ±0.1 V (gain = 100), ±1 V (gain = 10) and ± 10V (gain = 1).

The DAQP card supports sampling rates up to 100 kHz with either 12 or 16-bit resolution. Equipped with a data FIFO of 2048 samples, the DAQP card can achieve high speed data acquisition under various operating platforms including MS-DOS®, Windows 3.xx and Windows 95®. Also equipped with a scan FIFO of the same size, the DAQP supports full speed, random order channel scanning and gain selection for all input channels including expansion channels. The DAQP card uses a 24-bit pacer clock and a programmable divide-by-2, by-10 or by-100 pre-scaler. The pacer clock can also be used with either an internal or external clock source. With the 10 MHz internal clock source, the pacer clock can generate accurate sampling rates from 0.006 Hz to 100 kHz. The DAQP card has 4 digital input and output channels, all TTL compatible, which may be used for process control or monitoring in addition to analog data acquisition.

Software drivers are provided that support various programming languages like Microsoft C/C++, Borland C/C++, Delphi, QuickBasic, Visual Basic for DOS and Turbo Pascal. Also included is a Dynamic Link Library (DLL) that supports programming languages under Microsoft Windows as well as the Visual Basic Controls (VBX). Omega includes it's user friendly data acquisition software: DaqEZ®, as well as turnkey software support for LabTech NoteBook®, SnapMaster®, LabVIEW® and TestPoint®.

2. Installation

2.1 Hardware Setup

Insert the DAQP card into any type II PCMCIA socket. All other configuration options are determined by the operating system.

2.2 Software Setup (Windows 95/98®)

An ".INF" file (DAQPCARD.INF) is provided on the root directory of the DAQSUITE CD-ROM for easy installation of the DAQP series card under Windows 95/98. The operating system uses the ".INF" file to determine what system resources are required by the card, searches for available resources to fill the requirements, configures the DAQP card hardware and then updates the hardware registry with an entry that allocates these resources.

2.2.1 Installing the DAQP Series Card

1. Insert the DAQP card in any available PCMCIA socket.
2. The first time a new PCMCIA type card is installed the "New Hardware Found" window opens. Windows 95/98 will automatically detect and configure the card. If the "New Hardware Found" window does not open, skip to the next section: "Viewing the PCMCIA Card Status".
3. Windows will ask for the CD-ROM that came with the device. Insert the CD, click "Next" to continue and then click "Finish".
4. Windows automatically browses the root directory on the CD for the INF file that defines configurations for the new hardware type found. The file name is not required. After searching the root directory, Windows will choose the correct file.
5. Your new PCMCIA card should now be configured. In the future, Windows will automatically recognize and configure this specific PCMCIA card type.

2.2.2 Viewing the DAQP Series Card Status

1. Double click the "My Computer" icon located on the Windows 95/98 desktop. This opens a folder showing the various drives, printers, etc. (This can also be done by clicking "Start", "Settings" and then "Control Panel").
2. Double click the "Control Panel" icon. This opens another folder with different system configuration utilities.
3. Double click the "PC card (PCMCIA)" icon. This opens the "PC Card (PCMCIA) Properties" window.
4. The "PC Card (PCMCIA) Properties" window shows the status of your computers PCMCIA sockets. The DAQP card should be listed in one of these sockets. To change the DAQP card configuration see the next section.

IMPORTANT:

If you are using Windows 95/98 to configure the DAQP card then ignore section 2.3 of this chapter. The Windows 95/98 operating system completely installs and configures the DAQP series card. Do NOT attempt to use the DAQP series Client Driver or Enabler to configure any DAQP series card under Windows 95/98.

2.2.3 Changing the Configuration of the DAQP Card

1. Double click the "My Computer" icon located on the Windows 95 desktop. Inside the "My Computer" folder, double click the "Control Panel" icon. This can also be done by clicking "Start", "Settings" and then "Control Panel".

2. Inside the "Control Panel" folder, double click the "System" icon so that the "System Properties" window opens. Select the "Device Manager" tab. Find the entry titled "Data_Acquisition" on the device list. Expand the entry by clicking the leading "+" sign or by double clicking the name.

3. From the expanded sub-list, choose the DAQP card to reconfigure (there may be only one entry) by double clicking it.

4. Select the "Resources" tab from the pop-up window. Click the resource type (either "Input/Output range" or "Interrupt Request") from the "Resource Setting" table and then click the "Change Settings ..." button. This opens the "Edit Input/Output Range" or " Edit Interrupt Request" window.

5. Change the value by clicking on the slider controls by the "value" list and then click OK to confirm the change, or CANCEL to discard it. Watch for possible conflicts shown in the "Conflict Information" box.

The only configuration parameters that can be changed for the DAQP card under Windows 95/98 are "Input/Output Ranges" and "Interrupt Request".

2.3 Software Setup (Windows 3.xx and MS-DOS®)

Two software configuration programs are provided with the DAQP card: a Client Driver named DAQP_CL.SYS and a card Enabler named DAQP_EN.EXE. Either one of these programs may be used to configure the card **but only one may be used at a time**. The table below highlights the differences between the Client Driver and the Enabler programs. (Detailed instructions for using the Client Driver and Enabler are discussed in Chapters 3 and 4 respectively).

Client Driver	Enabler
DAQP_CL.SYS	DAQP_EN.EXE
Interfaces to PCMCIA Card and Socket Services software (PCMCIA host adapter independent)	Interfaces directly to Intel 82365SL and other PCIC compatible PCMCIA host adapters
Allows automatic configuration of DAQP card upon insertion (Hot Swapping)	Does not support automatic configuration of DAQP card upon insertion (Hot Swapping)
Requires PCMCIA Card and Socket Services software	Does not require PCMCIA Card and Socket Services software

Table 2-1. Comparison Between Client Driver and Enabler

On systems with Card and Socket Services installed, the Client Driver is the preferred method of installation. To determine if Card and Socket Services software is installed, install the DAQP series Client Driver as discussed in Chapter 3. When loaded, the Client Driver will display an error message if Card and Socket Services software is not detected.

3. Using the Client Driver

3.1 Installing the Client Driver

For systems using MS-DOS and PCMCIA Card and Socket Services software, a Client Driver named “DAQP_CL.SYS” is provided to configure the DAQP series cards. PCMCIA Card and Socket Services software is not provided and must be purchased independently.

Some versions of Card and Socket Services dated before 1993 do not support general purpose I/O cards. After careful installation of the Client Driver, if the DAQP card still does not configure or operate properly, an updated version of Card and Socket Services software may be required. The following procedures are used to install the DAQP series Client Driver:

1. Copy the file DAQP_CL.SYS located in the PCMCIA\DOS\CLIENTS directory of the “DAQSUITE” CD-ROM onto the root directory of the system hard drive.
2. Using an ASCII text editor, open the system CONFIG.SYS file located in the root directory of the boot drive.
3. Locate the line in the CONFIG.SYS file where the Card and Socket Services software is installed.
4. AFTER the line installing the Card and Socket Services software, add the following line to the CONFIG.SYS file:

   DEVICE = drive:\path\DAQP_CL.SYS options

   where options are the DAQP series Client Driver command line options discussed on the following pages. (Path is only required if the user copies the Client Driver into a directory other than the root directory).
5. Save the CONFIG.SYS file and exit the text editor.
6. Insert the DAQP card into one of the system PCMCIA slots.

   NOTE: Since the DAQP series Client Driver supports "Hot Swapping", it is not necessary to have the DAQP card installed when booting the system. However, by inserting the card before booting, the Client Driver will report the card configuration during the boot process and thereby verify changes made to the CONFIG.SYS file.
7. Reboot the system and note the message displayed when the Client Driver is loaded. If the Client Driver reports an “invalid command line option”, correct the entry in the CONFIG.SYS file and reboot the system. If the Client Driver reports “Card and Socket Services not found”, then either Card and Socket Services software must be installed on the system or the DAQP series Enabler program must be used to configure the card, (see Chapter 4). If the Client Driver reports the desired card configuration, the installation process is complete and the DAQP card may be removed and inserted from the system as desired. On each insertion into the PCMCIA socket, the DAQP card will automatically be reconfigured to the specified settings.

3.2 Client Driver Command Line Options

The DAQP series Client Driver accepts up to eight command line arguments from the user to determine the configuration of the DAQP card. If any arguments are provided, the Client Driver will attempt to configure any DAQP card with the options specified in the order they are entered on the command line. Each argument must be enclosed in parenthesis and must be separated from other arguments by a space in the command line. Inside an argument, a comma (no space) should be used to separate the parameters from each other if there are two or more parameters. Within each argument, any or all of the following parameters may be specified:

(b *address)* Specifies the base I/O address of the DAQP card in hexadecimal. "*Address"* must be in the range 100H - 3F8H and must reside on an even 8-byte boundary ("*address"* must end in 0 or 8). If this option is omitted, a base address will be assigned by Card and Socket Services software.

(i *irq*) Specifies the interrupt level (IRQ) of the DAQP card in hexadecimal. "*Irq"* must be one of the following values: 3, 4, 5, 7, 9, 10, 11, 12, 14, 15 or 0 if no IRQ is desired. If this option is omitted, an interrupt level will be assigned by Card and Socket Services software.

(s *socket)* Specifies the PCMCIA socket number to configure. *"Socket"* must be in the range 0 - 15. If this option is omitted, the configuration argument will be applied to any DAQP card inserted into any socket(s) in the system.

3.3 Client Driver Installation Examples

With the Client Driver, the user may specify a list of selections (in the form of command line arguments) for the configuration of the DAQP series cards. The Client Driver scans this list from left to right until it finds a selection that is currently available in the system. If none of the preferred selections are available, the Client Driver requests a configuration from Card and Socket Services software.

Example 1: DEVICE = C:\DAQP_CL.SYS

In example 1, no command line arguments are specified. The Client Driver will configure the DAQP card into ANY socket with a base address and IRQ level assigned by Card and Socket Services.

Example 2: DEVICE = C:\DAQP_CL.SYS (b300)

In this example, a single command line argument is provided. The Client Driver will attempt to configure a DAQP card inserted into ANY socket with a base address of 300H and an IRQ level assigned by Card and Socket Services. If the base address 300H is not available, the DAQP card will NOT be configured.

Example 3: DEVICE = C:\DAQP_CL.SYS (s0,b300,i5)

Example 3 is also a single command line argument. The Client Driver will attempt to configure the DAQP card inserted in socket 0 at base address 300H and IRQ level 5. If either address 300H or IRQ 5 are unavailable, the card will NOT be configured. In addition, the Client Driver will NOT configure any DAQP card unless inserted into socket 0.

Example 4: DEVICE = C:\DAQP_CL.SYS (b300,i5) (i10) ( )

Three command line arguments are provided in this example. The Client Driver will first attempt to configure a DAQP card inserted into any socket with a base address 300H and IRQ level 5. If either address 300H or IRQ 5 are unavailable, the Client Driver will proceed to the second command line argument and attempt to configure the card with a base address assigned by the Card and Socket Services and IRQ level 10. If IRQ 10 is also unavailable, the Client Driver will then go to the third command line argument and attempt to configure it with a base address and an IRQ level assigned by Card and Socket Services.

Example 5: DEVICE = C:\DAQP_CL.SYS (b300,i5) ( ) (i10)

The difference between examples 5 and 4 is the order of the second and third command line arguments. The Client Driver will first attempt to configure a DAQP card inserted into any socket with a base address 300H and IRQ level 5. If either address 300H or IRQ 5 are unavailable, the Client Driver will proceed to the second command line argument and attempt to configure the card with a base address and IRQ level assigned by Card and Socket Services. Since the second command line argument includes all available address and IRQ resources, the third command line argument will never be reached. The user must ensure the command line arguments are placed in a logical order.

Example 6: DEVICE = C:\DAQP_CL.SYS (s0,b300,i5) (s1,b310,i10)

There are two command line arguments in example 6, which is desirable in systems where two or more DAQP cards are to be installed. The Client Driver will attempt to configure the DAQP card in socket 0 with base address 300H and IRQ level 5. If there is a DAQP card in socket 1, it will be configured with base address 310H and IRQ 10. This allows the user to force the card addresses and IRQ settings to be socket specific as required by software or cable connections. If the requested resources are not available, the DAQP cards will not be configured.

3.4 Common Problems

3.4.1 Generic Client Drivers

Many Card and Socket Services packages include a generic client driver (or SuperClient) which configures standard I/O devices. If one of these generic client drivers is installed, it may configure the DAQP card and cause the DAQP series Client Driver to fail installation. If this is the case, the operation of the generic client driver can be modified so that it will not configure the DAQP card. Place the DAQP series Client Driver command line before the generic client driver command line in the CONFIG.SYS file. Consult the Card and Socket Services documentation for availability and details of this feature.

3.4.1 Available Resources

One function of Card and Socket Services software is to track which system resources (memory addresses, I/O addresses, IRQ levels, etc.) are available for assignment to inserted PCMCIA cards. Sometimes, however, the Card and Socket Services assumes or incorrectly determines that a particular resource is unavailable when it actually is available. Most Card and Socket Services generate a resource table, typically in the form of an ".INI" file, which the user can modify to adjust the available system resources. Consult the Card and Socket Services documentation for the availability and details of this feature.

3.4.2 Multiple Configuration Attempts

Some Card and Socket Services have a setting which aborts the configuration process after a single configuration failure (such as a configuration request for an unavailable resource). The user should change this setting to allow for multiple configuration attempts. Consult the Card and Socket Services documentation for the availability and details of this feature.

3.4.3 Older Versions of Card and Socket Services

Some versions of Card and Socket Services dated before 1993 do not support general purpose I/O cards like the DAQP series cards. If after careful installation of the DAQP Client Driver, the DAQP card still can not be configured or operated properly, an updated version of Card and Socket Services may be required.

3.5 After Completing Configuration

The DAQP card is now configured and ready for use. Depending on the type of application software to be used, the user may wish to review one or more of the following:

1. Chapter 5 of this document provides basic theory of operation for users that wish to learn technical details about the operation of the DAQP card.
2. For users that want to program direct I/O transfers to the DAQP card's register set, Chapter 7 provides an address map and a detailed description of each register.
3. Users that wish to write custom application software without programming the DAQP card directly should consult the DAQDRIVE® software reference manual. DAQDRIVE provides a library of data acquisition subroutines for various data acquisition cards and is included free of charge with the DAQP card.
4. For turnkey data acquisition software such as LabTech NoteBook®, SnapMaster®, LabVIEW® and TestPoint®, consult the documentation provided by the software manufacturer.

4. Using the Enabler

For systems that are not operating PCMCIA Card and Socket Services software, the DAQP series card includes an Enabler program to enable and configure the DAQP series card. This Enabler, DAQP_EN.EXE, will operate in any DOS system using an Intel 82365SL or PCIC compatible PCMCIA host adapter including the Cirrus Logic CL-PD6710/6720, the VLSI VL82C146 and the Vadem VG-365.

In order to use the DAQP series Enabler for DOS, the system must NOT be configured with Card and Socket Services software. If Card and Socket Services software is installed, the Enabler may interfere with its operation and the devices it controls. Therefore use either the DAQP series Client Driver or Enabler exclusively.

The DAQP series Enabler does not support automatic configuration of PCMCIA cards upon insertion, more commonly referred to as “Hot Swapping”. This means the card must be installed in one of the system's PCMCIA sockets before executing DAQP_EN.EXE. If more than one adapter is installed in a system, the Enabler must be executed separately for each card. Furthermore, DAQP_EN.EXE should be executed to release the resources used by the card before it is removed from the PCMCIA socket. Since PCMCIA cards do not retain their configuration after removal, any card removed from the system must be reconfigured with the Enabler after being reinserted into it’s PCMCIA socket.

The Enabler requires a region of high DOS memory when configuring the DAQP card. This region is 1000H (4096) bytes long and by default begins at address D0000H (this may be changed by the “W” option as will be described later). If a memory manager such EMM386, QEMM or 386MAX is installed on the system, this region of DOS memory must be excluded from the memory manager’s control (normally by using the “x” switch). Consult the documentation provided with the memory manager software for instructions on how to exclude this memory region.

The following procedures are used to install the DAQP series Enabler:

1. Copy the file DAQP_EN.EXE located in the PCMCIA\DOS\ENABLERS directory of the “DAQSUITE” CD-ROM onto the root directory of the system hard drive.
2. Using an ASCII text editor, open the system's CONFIG.SYS file located in the root directory of the boot drive.
3. Add the following line to the CONFIG.SYS file:

   DEVICE = drive:\DAQP_EN.EXE (options)

   where (options) are the DAQPA series Enabler command line options discussed on the following pages.
4. Save the CONFIG.SYS file and exit the text editor.

5. Insert the DAQP card into one of the system PCMCIA slots.
   NOTE: Since the DAQP series Enabler does not support "Hot Swapping", it is necessary to have the DAQP card installed when booting the system.
6. Reboot the system and note the message displayed when the Enabler is loaded. If the Enabler reports the desired card configuration, the installation process is complete.

4.1 Enabler Command Line Options

To configure a DAQP series card in the system, the Enabler requires one command line argument from the user to determine the configuration. This argument must be enclosed in parenthesis. Within the argument, a comma (no space) must be used to separate the parameters from each other if there are two or more parameters. The following parameters may be specified in the command line argument:

(s *socket*) Specifies the PCMCIA socket number to configure. "*Socket*" must be in the range 0 - 15. This option is always required.

(b *address)* Specifies the base I/O address of the DAQP card in hexadecimal. "*Address*" must reside on an even 8-byte boundary ("*address*" must end in 0 or 8). This option is required if the "r" option is not used.

(i *irq*) Specifies the interrupt level (IRQ) of the DAQP card in hexadecimal. "*Irq*" must be one of the following values: 3, 4, 5, 7, 9, 10, 11, 12, 14, 15, or 0 if no IRQ is desired. This option is required if the "r" option is not used.

(w *address)* Specifies the base address of the memory window required to configure the DAQP card. Set "*address*" = D0 for a memory window at D0000, = D8 for a memory window at D8000, etc. Valid settings for address are C8, CC, D0, D4, D8, and DC. If omitted, "*address*" = D0 is assumed.

(r) Instructs the Enabler to release the resources previously allocated to the DAQP card. When this option is used, (b *address*) and (i *irq*) options will be ignored. Therefore, do NOT use this option when initially configuring the DAQP card.

4.2 Enabler Examples

Example 1: DEVICE=C:\DAQP_EN.EXE

No command line argument is specified. The Enabler will report an error and display the proper usage of the Enabler.

Example 2: DEVICE=C:\DAQP_EN.EXE (s0,b300,i5)

In this example, the Enabler will configure the DAQP card in socket 0 with a base address 300H and IRQ level 5 using a configuration memory window at D0000H.

Example 3: DEVICE=C:\DAQP_EN.EXE (i10,b310,s1)

In example 3, the Enabler will configure the DAQP card in socket 1 with a base address at 310H and IRQ level 10 using a configuration memory window at D0000H. Note the parameter order is not significant.

Example 4: DEVICE=C:\DAQP_EN.EXE (s0,b300,i5,wCC)

Here the Enabler will configure the DAQP card in socket 0 with a base address at 300H and IRQ level 5 using a configuration memory window at CC000H.

Example 5: DEVICE=C:\DAQP_EN.EXE (s0,r)

DEVICE=C:\DAQP_EN.EXE (s0,r,b300,i5)

These two command line arguments are equivalent because of the “r” option. The Enabler will release the configuration used by the DAQP card in socket 0 using a configuration memory window at D0000H.

Example 6: DEVICE=C:\DAQP_EN.EXE (s0,r,wC8)

Here the Enabler will release the configuration used by the DAQP card in socket 1, using a configuration memory window at C8000H.

4.3 Common Problems

4.3.1 Memory Range Exclusion

The Enabler requires a region of high DOS memory when configuring a DAQP card. This region is 1000H (4096) bytes long and by default begins at address D0000H (this default address can be changed by using the "W" option). If a memory manager such as EMM386, QEMM or 386MAX is installed on the system, this region of DOS memory must be excluded from the memory manager's control (normally by using the "x" switch). Consult the documentation provided with the memory manager software for instructions on how to exclude this memory region. Furthermore, some systems use the high memory area for ROM shadowing to improve overall system performance. For the Enabler to properly operate, any ROM shadowing must be disabled in the address range specified for the configuration window. This can usually be completed by using the system's CMOS setup utility.

4.3.2 Socket Numbers

The Enabler requires that the socket number be specified for the DAQP card to be configured. The DAQP card must be inserted into the socket before executing the Enabler. For the DAQP series Enabler, the lowest socket number is always designated as socket 0 and the highest socket number as N-1, (assuming there are N sockets available). Some vendors number their sockets from 1 to N. In that case, the vendor socket number minus 1 should be used in the "s" option for the DAQP series Enabler.

4.3.3 Card and Socket Services Software

In order to use DAQP series Enabler for DOS, the system must NOT be configured with Card and Socket Services software. If Card and Socket Services software is installed, the Enabler may interfere with its operation and the devices it controls.

4.4 After Completing Configuration

The DAQP card is now configured and ready for use. Depending on the type of application software to be used, the user may wish to review one or more of the following:

1. Chapter 5 of this document provides basic theory of operation for users that wish to learn technical details about the operation of the DAQP series card.

2. For users that want to program direct I/O transfers to the DAQP card's register set, Chapter 7 provides an address map and a detailed description of each register.

3. Users that wish to write custom application software without programming the DAQP card directly should consult the DAQDRIVE® software reference manual. DAQDRIVE provides a library of data acquisition subroutines for various data acquisition cards and is included free of charge with the DAQP card.

4. For turnkey data acquisition software such as LabTech NoteBook®, SnapMaster®, LabVIEW® and TestPoint®, consult the documentation provided by the software manufacturer.

5. Theory of Operation

The DAQP card consists of 8 differential or 16 single-ended analog input channels. The A/D converter, either 12 -bit or 16-bit, can be operated at a top speed of 100,000 samples per second, (10 ms per sample). The A/D converter uses left-justified 2's complement coding. For the 16-bit version, the output ranges from -32768 to 32767. The 12-bit version is structured so that it's contents occupy the most significant 12 bits, padding the least significant 4 bits with all zeros to make a 16-bit output word for each converted input sample.

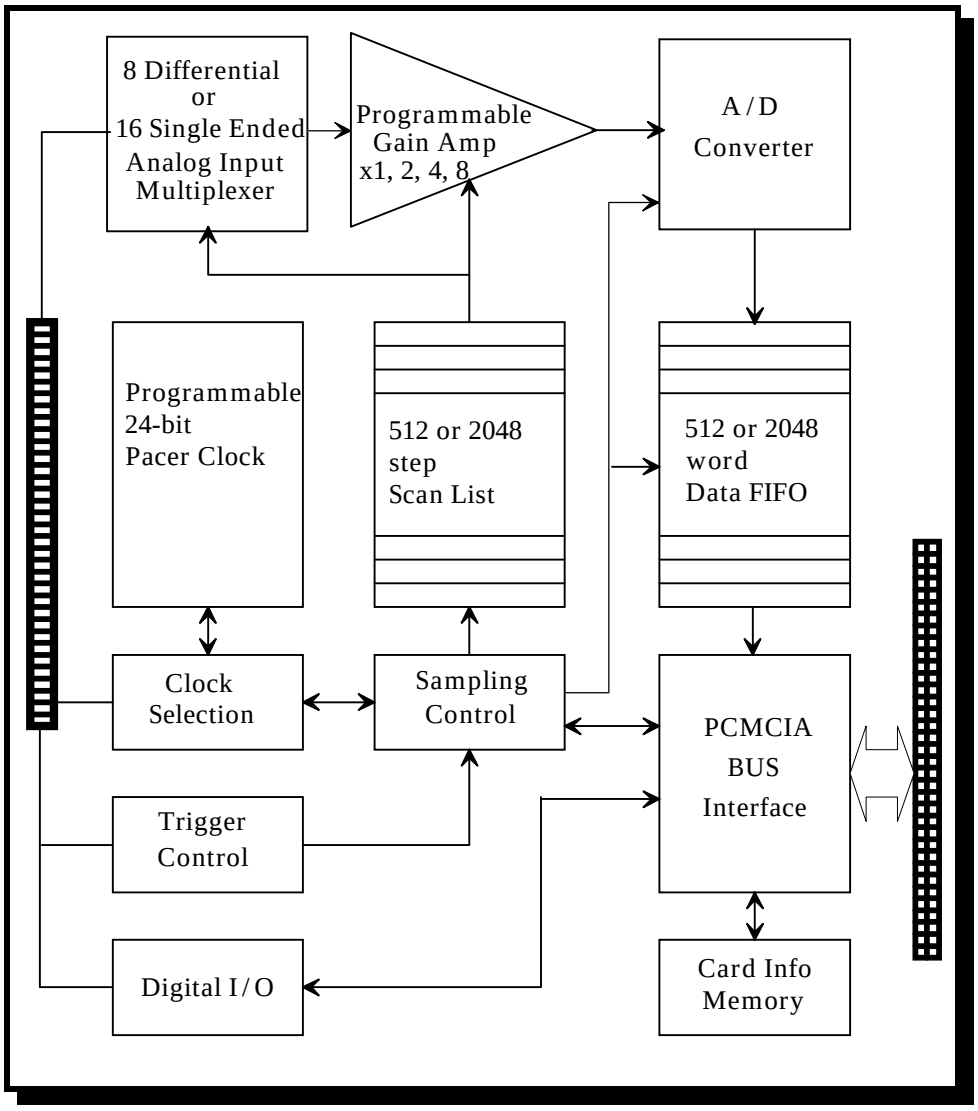

Figure 5-1. DAQP Data Acquisition System Block Diagram

The DAQP card can be operated as an I/O device, occupying eight consecutive bytes in the I/O address space. It can also be configured to operate via memory mapped I/O. The DAQP fully complies with PCMCIA standard 2.10 as a type II card. The card has no jumpers or DIP switches. All the configurable features are software programmable.

Functionally, the DAQP card consists of the following components: the DC/DC power supply, analog input multiplexer, programmable gain control amplifier, A/D converter, data FIFO, scan list FIFO, trigger control circuit, pacer clock, interrupt & status registers, digital I/O register and associated control circuits.

5.1 DC/DC Power Supply

The DAQP card uses a standard +5 volt digital input power supply from the PCMCIA connector to generate the ±15 volt power supplies for the analog front end and the +5 volt power supply for the A/D converter. The DC/DC converter uses 140 mA, 78% of the 180 mA total load current, from the digital input power supply to generate the necessary voltages.

According to the PCMCIA standard, any card that draws more than 100 mA must not be automatically turned on upon insertion until it is intentionally accessed by writing to the card configuration and option register (or its allocated I/O space). The DAQP card supports this specification by providing a unique power down mode control. When the card is first powered up or after a reset, the DC/DC converter is turned off, so that only the digital portion of the DAQP card is up and running. This requires only 40 mA from the digital input +5 volt power supply. The user has the option of reading the card information memory, where the maximum power consumption is listed for reference, and then decide whether or not to "wake up" the card. If required, the card can be set to full power mode immediately when it's PCMCIA configuration and option register (COR) is written by the software.

After the card is set for full power mode for the first time by writing the PCMCIA configuration and option register, it can then be set to power down mode by writing a '1' into bit 2 (the power down bit) of the PCMCIA auxiliary control register. Refer to Chapter 6 for more information about the COR.

5.2 Analog Input Multiplexer

Differential or single-ended configuration is determined by bit 6 of the high byte in the scan list register. '1' selects differential input, while a '0' selects single-ended input. Expansion cards will only support single-ended channels. It is strongly recommended that single-ended or differential selection be uniform for all internal channels (e.g., all 8 channels as differential or all 16 channels as single-ended). Although it is possible to have some channels configured as single-ended and others as differential, doing so may cause confusion and unexpected signal errors.

With differential configuration, there are 8 channels. However, if the user specifies channels 8 to 15 in a differential configuration, it will short the inputs to ground for system offset measurement. The readings taken under such a circumstance can be used for offset correction.

The input multiplexers have built-in protection against over-voltage when the board is at full power AND when it is powered down. The protection mechanism will isolate the input from the rest of the board, as long as the input voltage is within the protection range of ± 30 volts.

5.3 Programmable Gain Control Amplifier

The DAQP-12 and DAQP-16 cards have an internal gain of 1, 2, 4 or 8; and the DAQP-12H has an internal gain of 1, 10, 100 or 1000. The gain can be changed "on the fly" when scanning from channel to channel by changing the configuration of the programmable gain instrumentation amplifiers. The internal gain selection is specified by the scan list entry, bits 4 and 5 of the high byte. The contents of these two bits will determine the gain of the analog front end.

The settling time of the analog front end meets speed requirements, however, if the amplifier is saturated it may need more time to recover. This can cause distortion at the input signal to the A/D converter. It is recommended that amplifier saturation be avoided by using a low gain and attenuating the input signal whenever possible.

5.4 Scan List Register

One entry to the scan list register contains a 16-bit word or two 8-bit bytes. It specifies the internal channel and gain selection in the high byte or MSB, and the external channel and gain selection in the low byte or LSB, in addition to other control and configuration settings. The external selections are used for expansion card channels (up to 256), while the internal selections are for channels on board the DAQP card. Expansion cards are not included as part of the DAQP series data acquisition system, however, they can be purchased separately from your vendor.

The number of entries in the scan list ranges from 1 to 2048. There are no dependencies implied among the entries of the scan list. The user may choose any valid gain combination for any channel, internal or external. Channels can be scanned in any order required, repeated or not, with the same or different gain for each entry.

The scan list has to be flushed before programming to guarantee the integrity of each entry. There must be an even number of bytes programmed into the scan list, with the low byte sitting at an even offset followed by the high byte, otherwise the channel scan result will be unpredictable.

It is strongly recommended that the differential/single-ended control bit (bit 14, MSB) be programmed the same for all the entries in the scan list. Single-ended configuration should be selected if there are expansion cards connected to the DAQP card. The synchronous sample hold bit (bit 6, LSB) is reserved for expansion cards.

The first channel flag (bit 7, LSB) has to be set for the first (and ONLY the first) entry of the scan list. The DAQP card hardware relies on this bit to tell the end (or the start) of the scan. During normal operations, the DAQP card starts one scan when triggered, (software or TTL trigger in one-shot mode or sampling pulse triggers from the pacer clock in continuous mode). During the scan, each entry in the scan list will be processed until it finds the entry that has the first channel flag set to '1'. The hardware then stops scanning and waits for the next trigger. The scan will continue indefinitely if none of the list entries has the flag set to '1'. On the other hand, if more than one entry has the flag set to '1', the scan list will then be chopped

into pieces. Each piece will require a trigger to be scanned. Should the flag be set to '1' on an entry other than the first, a "starting offset" will be introduced to the scan list. Channel scanning will start from the entry with the flag set to '1', run through the list, turn around and end at the one before it. Although this may be useful for diagnosis or special applications, it is the abnormal way of setting the first channel flag and should be avoided unless absolutely necessary.

5.5 Trigger Circuit

The DAQP card can be triggered by software, an external TTL signal or the pacer clock. For the external TTL trigger, an active trigger edge can be selected for either the low-to-high or high-to-low transition.

In one-shot trigger mode, one trigger, either internal or external, will start one and only one scan of all channels specified in the scan list. (The pacer clock has no effect in this mode although it is good practice to program the pacer clock with a divisor greater than 2). Multiple scans can be initiated by issuing multiple triggers.

In continuous trigger mode, the software or TTL trigger initiates a series of scans. The first scan begins immediately on receiving a trigger, while the rest are carried out each time the pacer clock fires. The process will continue until an A/D stop command is received.

If the internal trigger (or software trigger) is selected, the trig/arm command will serve as a trigger when received by the DAQP card. For the external trigger source, the same command will be taken as an arm command, which arms the DAQP card so that the first proper trigger edge following the arm command will serve as the trigger. Unexpected edge transitions during the trigger source configuration are totally ignored if the DAQP card is not armed.

5.6 A/D Converter and Data FIFO

The DAQP card always assumes a bipolar input range of ±10V if the gain is one. The output data format will always be in 2's complement (and left justified for 12-bit versions). The data acquisition time of the A/D converter is 2µs while it's conversion time is no more than 8µs. The output of the A/D converter is fed into a data FIFO providing data buffering of up to 2048 samples. The A/D converter, once triggered, will complete conversion for every analog input channel in the scan list at the specified scan speed and then feed the results into the data FIFO. In between scans, the DAQP card waits until another trigger is received (one-shot mode) or the pacer clock fires (continuous mode).

The data FIFO has two programmable thresholds, one for almost full and the other for almost empty. The DAQP card uses the almost full threshold and ignores the other one. The data FIFO should always be flushed prior to using the arm/trig command to start data acquisition. When the FIFO is flushed or emptied by the host reading its content, the FIFO empty flag will be set. As long as there are samples left in the data FIFO, the empty flag will be cleared. When the number of data samples in the FIFO becomes greater than the programmed almost full threshold, the almost full flag is set. When the number becomes less than or equal to the specified almost full threshold, the flag will be cleared. On power up or reset, the threshold is

defaulted at 7 bytes to full (3.5 samples). Correct setting of the threshold will help achieve optimal performance of the card.

When the FIFO is full, the full flag will be set, and no more samples can be written into the FIFO. At the end of each scan, the DAQP card will set the data lost flag if the data FIFO is already full. This flag is not set before or during the scan, but at the end of it. Once the data lost flag is set, it will not clear until the status register is read.

5.7 Interrupt and Status

The DAQP card has two interrupt sources, the end-of-scan (EOS) interrupt and the FIFO threshold interrupt. The control register (base + 2, write only) has two bits to enable or disable either one of the interrupts independently. However, it is strongly recommended that the two interrupts be used exclusively.

When the EOS interrupt is enabled, an interrupt is sent to the host at the end of each scan of the channel list. If there is only one channel in the scan list, the EOS interrupt is reduced to an EOC (end-of-conversion) interrupt. The FIFO threshold interrupt, when enabled, is sent to the host when the almost full flag is set. The host then uses the "string input" instruction to move a block of samples from the FIFO. The EOS and FIFO threshold event bits in the status register (base + 2, read only) and will be set whenever the corresponding event happens. These bits can be used for indicating the source of the interrupt. Once set, the event bits will not be cleared until the host reads the status register.

5.8 Digital I/O

The DAQP card has one digital input port (base + 3, read only) of four bits (bits 0-3) and one digital output port (base + 3, write only) of four bits (bits 0-3). The output port is latched, while the input port is not. Four input lines are connected to the digital input port, each representing one bit in the port. When reading the digital input port, the CURRENT status of the digital input lines are returned to the host.

All four input lines are shared with other functions. Bit 0 is shared as the external trigger input, while bit 2 is shared as the external clock input. Bits 1 and 3 are taken over as the external gain selection lines if there is an expansion card(s) connected and the expansion bit in the control register is set to '1'. In this case, the digital output lines are driven by the external channel selection bits of the current scan list entry. Otherwise, they will be connected to the latched bits 0-3 of the digital output port. The current status of the digital input lines will always be returned when the host reads the digital input port regardless of whether the lines are shared or not.

5.9 A/D State Machine

The DAQP card has an internal state machine that controls A/D operation. The state machine defaults to S0 after power up or reset. The normal state flow would be first S0 to S3, initiated by a scan list (queue) flush command (RSTQ). Then the queue must be programmed by writing into the queue (base + 1). With the queue being programmed, the next step is moving the state machine from S3 back to S0. This is done by issuing a flush data FIFO command (RSTF), which sets up the gain and channel selections for the first channel in the scan list and then waits for a trigger to start the scan. When the trigger (ADCLK) comes, the state machine moves from S0 to S1 and then A/D conversion is started. The state machine will wait at S2 until the conversion is completed. It then moves to S4, where the A/D conversion result is written into the data FIFO. The scan rate is determined by the time the state machine moves from S1 to S4, which can be programmed as either 10, 20 or 40 µs. If there are more channels left in the scan list, the state machine will skip to S1 for another conversion loop. Otherwise it will return to S0, waiting for another trigger (or a sampling pulse from the pacer clock if in continuous trigger mode). Any time during data acquisition, an A/D stop command will stop the data acquisition by moving the state machine back to S0.

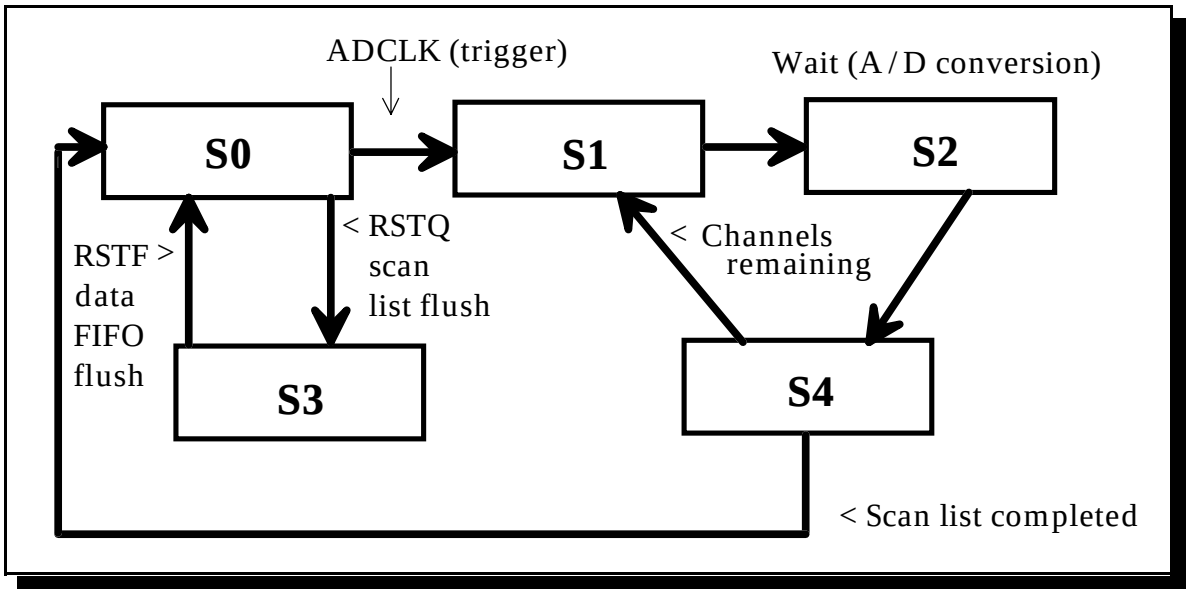

Figure 5-3. Transition Diagram of A/D Conversion Process

It is important that the sequence of S0-S3-S0 be followed as described above. The user must issue two commands to the DAQP card: the flush scan list command (RSTQ) and the flush data FIFO command (RSTF). This guarantees that the scan list and the data FIFO are flushed properly for the expected data acquisition. Once the flush data FIFO command is issued, the DAQP card will prepare the first channel in the scan list and then return to state S0 waiting for the first trigger. Anytime the data FIFO is flushed, the default threshold setting will be restored (7 bytes to full) by the hardware. The data FIFO threshold should always be programmed after flushing if the required threshold is different from the default threshold.

6. PCMCIA Interface

The information in this section is provided for those who need low level PCMCIA interface details for the DAQP card. The client driver or enabler that comes with the DAQP card will be sufficient for most applications.

The DAQP card performs data acquisition for all host computers equipped with a version 2.10 compliant PCMCIA interface. The DAQP card has a form factor of type II (5 mm thick). The card is highly flexible with respect to addressing and interrupt level use. It can be configured either as a memory only interface or as an I/O interface and can be powered up or down with the help of PCMCIA card and socket services. The DAQP card provides a single interrupt that can be routed to any system interrupt via the PCMCIA socket controller.

There are two sets of registers on the DAQP card: the program registers and the configuration registers.

Program registers fall under program control and belong to the DAQP card. The I/O location of these registers is controlled by the PCMCIA socket configuration and by the contents of the PCMCIA configuration registers.

The configuration registers are as those defined in the PCMCIA 2.10 specification and are located in the DAQP card's configuration space at offset 8000H. The configuration space also contains the Card Information Structure (CIS) which is located at offset 0000H. The CIS memory contains information about the DAQP card as defined by the PCMCIA 2.10 specification. It is recommended that configuration and power up/down control of the DAQP card be carried out through the standard card and socket services although an enabler can be used to complete these tasks.

Two PCMCIA configuration registers are supported by the DAQP card, (see Table 6-1): the Configuration Option Register and the Card Configuration and Status Register.

Offset	Access	Description
0x8000	R/W	Configuration Option Register
0x8002	R/W	Card Configuration and Status Register

Table 6-1. PCMCIA Configuration Registers

6.1 Configuration and Option Register (COR)

Bits 7 and 6 of the Configuration Option Register are defined by the PCMCIA standard as the SRESET and the LevlREQ Bits. A '1' written into the SRESET bit puts the card in reset state, while a '0' moves it out of reset state. In reset state, it behaves as if a hardware reset is received from the host. The LevlREQ bit controls the type of interrupt signal generated by the DAQP card. Setting the Configuration Index bits to '0' makes the DAQP card a memory only card (accessed only by memory read/write operations), while setting it to '1' enables the card for standard I/O. Table 6-2 lists the COR bit definition.

Bit	Name	Description
7	SRESET	1 = Put the card into reset state 0 = Get out of reset state
6	LevlReq	1 = Level mode interrupt 0 = Edge mode interrupt
5-0	Index Bits	000000 = Memory mode 000001 = I/O mode

Table 6-2. COR Bit Definition

6.2 Card Configuration and Status Register (CCSR)

The DAQP card uses two bits in this register. When bit 1 is set to '1', it indicates a pending interrupt. The bit will remain as '1' until the interrupt source is cleared. Bit 2 is used for power down control. Setting a '1' at this bit will put the card into power down mode, while a '0' brings it back to full power mode. The remaining bits are not used.

Bit	Name	Description
7--3	Not Used	Reserved, all '0' when writing and reading
2	PwrDwn	1 = Power down mode 0 = Full powered mode
1	Intr	1 = Interrupt pending 0 = No interrupt pending
0	Reserved	Reserved as '0'

Table 6-3. CCSR Bit Definition

7. I/O Registers

The DAQP card uses eight consecutive I/O locations within the system I/O address space. The base address of the adapter is determined by the Client Driver or Enabler as discussed in Chapters 3 and 4. The eight I/O locations are used by the DAQP card as summarized in the following table.

Address Lines (A2A1A0)	I/O Address	Port Access	Register Description
000	base + 0	Read/Write	Data FIFO
001	base + 1	Write Only	Scan List (Queue)
010	base + 2	Write Read	Control Register Status Register
011	base + 3	Write Read	Digital Output Register Digital Input Register
100	base + 4	Write Only	Pacer Clock, low byte
101	base + 5	Write Only	Pacer Clock, middle byte
110	base + 6	Write Only	Pacer Clock, high byte
111	base + 7	Write Only	Auxiliary Control Register

Table 7-1. DAQP Series Card Address Map

All registers are 8-bits wide and each is discussed in detail in the following sections.

7.1 Data FIFO Register (base + 0)

Note: Although the data FIFO register is 8 bits wide, it is strongly recommended that the register be accessed as a 16 bit word to guarantee integrity. The low byte (LSB or the least significant byte) should always be accessed first, followed by the high byte (MSB or the most significant byte).

The data FIFO register is considered as the access port to the data FIFO, which holds up to 2048 data words of the A/D conversion results. The port is also used for programming the data FIFO thresholds, as explained later in this section.

Two consecutive bytes should be read from or written into the port each time it is accessed. The following table illustrates bit allocation.

--	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LSB	D7	D6	D5	D4	D3	D2	D1	D0
MSB	D15	D14	D13	D12	D11	D10	D9	D8

Table 7-2. Data FIFO Register Bit Allocation

7.1.1 Data FIFO Operation Modes

Depending on the mode of operation, the 16-bit word read from or written into the register has different meanings, as described in the following table.

Mode	Selection Bit	A/D	Access	Operation
0	0, threshold	Idle	Read Write	Verify data FIFO threshold Program data FIFO threshold
1	1, data FIFO	Idle	Read Write	Read data FIFO Write data FIFO (diagnosis)
2	0, threshold	Run	Read Write	Verify data FIFO threshold Not allowed
3	1, data FIFO	Run	Read Write	Read data FIFO Not allowed

Table 7-3. Data FIFO Operation Mode

The “selection bit” is also called the “program/access” control bit, as defined in the auxiliary control register (base + 7). Mode 0 is the FIFO program mode, under which the two consecutive words (four bytes) written into the register address will set the almost full and almost empty thresholds (in bytes). The first word specifies the almost empty threshold, (not used, can be set to anything), while the second word determines the almost full threshold. The threshold should be set to a value from 1 to FIFO size minus 1. (Default is set to 7 at reset or power up). Refer to Table 7-4 for FIFO threshold settings.

Threshold	Default	Threshold Range	Suggested Value
Almost Empty	7	Irrelevant	Irrelevant
Almost Full	7	1..1023	512

Table 7-4. Data FIFO Threshold Setting

Mode 1 is FIFO test mode, in which data bytes will be written into the data FIFO and read back from it. The FIFO flags (empty, almost full, and full) will change according to the data bytes available in the data FIFO and the configured threshold.

Mode 2 should be avoided. The data bytes can not be written into the FIFO under this mode, while the bytes read from the FIFO will be the same as in mode 0.

Mode 3 is data transfer mode. Data bytes will be written into the FIFO by the A/D converter. The data byte read from the address is the first available byte in the data FIFO if it is not empty. If the FIFO is empty then the most recent byte written into the FIFO will be returned. The data FIFO register is read-only under this mode therefore the user cannot write data bytes into the data FIFO through I/O instructions.

7.1.2 Mode Setting

The FIFO operation mode setting is always initiated by the data FIFO flush command with the access/program bit set to '0' (bit 0 at base + 7) before data acquisition is started. This will set mode 0 (threshold setting mode). After the threshold is programmed or verified, set the bit to '1' so the following read/write operation to the FIFO will be data access operation.

The DAQP card is in idle mode before it is triggered into run mode. For one-shot operation, the DAQP card will be set to run mode after it receives the trigger signal. It will not return to idle mode until the specified scan list is completed or an A/D stop command is received. For continuous trigger operation, the DAQP card will stay in run mode after being triggered until an A/D stop command is received.

7.1.3 FIFO Flags

When reading the register under mode 1 or 3, the first available data byte from the data FIFO will be returned if it is not empty, otherwise the returned byte is not defined. The FIFO full flag will be cleared after the data FIFO register is read provided there are no more data bytes written into the FIFO by the A/D converter under mode 1 or 3. The same will happen to the FIFO almost full flag if the data bytes available in the FIFO are less than the almost full threshold. The FIFO empty flag will be set immediately after the last byte is read from the FIFO. FIFO size is measured in bytes (4096). Table 7-5 lists the FIFO flag status.

Data bytes in FIFO	Empty	Almost Full	Full
0	True	False	False
1 to (Threshold - 1)	False	False	False
Threshold to (FIFO size - 1)	False	True	False
FIFO size (either 1024 or 4096)	False	True	True

Table 7-5. Data FIFO Flag Status

7.2 Scan List Queue Register (base + 1)

The Scan List Queue Register is considered the access port to the scan list queue which can hold up to 2048 entries (each has two bytes). Each entry specifies an analog input channel and it's associated gain as well as other settings. The bit definition of an entry to the scan list queue is explained in Table 7-6.

Note: Although the scan list queue register is 8 bits wide, it is required that the register be accessed as a 16 bit word to guarantee integrity. The low byte (LSB or the least significant byte) should always be accessed first, followed by the high byte (MSB or the most significant byte).

Bit	Byte	Definition	Explanation
15	MSB	Reserved	as 0
14	MSB	Analog input mode	1 / 0 : differential / single-ended
13-12	MSB	Internal gain selection	00 / 01 / 10 / 11 : 1 / 2 / 4 / 8 or 00 / 01 / 10 / 11 : 1 / 10 / 100 / 1000
11-8	MSB	Internal channel selection	0000..1111 : channel 0..15
7	LSB	Starting channel mark	Set to '1' for the 1st entry in the list Set to '0' for all the rest entries
6	LSB	Reserved	for expansion cards (as SSH)
5-4	LSB	External gain selection	00 / 01 / 10 / 11 : 1 / 2 / 4 / 8 (or 1 / 10 / 100 / 1000)
3-0	LSB	External channel selection	0000..1111 : channel 0..15

Table 7-6. Scan List Queue Entry Bit Definition

7.2.1 Scan List Queue Programming

The scan list queue must be programmed when the DAQP card is idle. Each queue entry contains two bytes as described above and the integrity of the entry must be guaranteed. (The scan list queue is write only). The queue should be flushed before writing into it. Refer to section 7.7: Auxiliary Control Register for information on scan list queue reset. The first entry of the queue should have bit 7 (LSB) set to '1' as the first channel mark. For the remaining entries, set the bit to '0'. The synchronous sample hold bit (LSB) is not used by DAQP card. It is reserved for the expansion cards.

Example 1.

Table 7-7 lists the required queue entries to specify a scan list of three single-ended internal channels: 0, 12, and 7; with a gain of 2 for channel 0 and a gain of 4 for channels 12 and 7:

Entry	Binary	Hex	Explanation
1	0001 0000 1000 0000	0180	Select channel 0, gain 2, 1st
2	0010 1100 0000 0000	2C00	Select channel 12, gain 4
3	0010 0111 0000 0000	2700	Select channel 7, gain 4

Table 7-7. Scan List Queue Programming Example 1

Example 2.

Table 7-8 lists the required queue entries to specify a scan list of 4 differential internal channels: 2, 1, 6 and 7; with gain of 1 for all channels:

Entry	Binary	Hex	Explanation
1	0100 0010 1000 0000	4280	Select channel 2, gain 1, 1st
2	0100 0001 0000 0000	4100	Select channel 1, gain 1
3	0100 0110 0000 0000	4600	Select channel 6, gain 1
4	0100 0111 0000 0000	4700	Select channel 7, gain 1

Table 7-8. Scan List Queue Programming Example 2

7.2.2 Channel Configuration

Bits 5 and 4 (LSB) in a queue entry specify the gain of the external expansion card for the external channel selected by bits 0-3 of the same byte. Each expansion card has up to 16 channels (0, 1, 2, ..., 15). Each channel may have a gain of 1, 2, 4 or 8 (DAQP-12/16) or 1, 10, 100 or 1000 (DAQP-12H). If there is no expansion card for the internal channel specified then the external channel and gain selection in the LSB will be ignored. However, the first channel mark on bit 7 should always be properly set. The internal channel is selected by bits 8-11 (MSB), while the internal gain for the selected channel is specified by bit 12 and 13 (MSB). The internal gain can only be 1, 2, 4 or 8. Bit 14 (MSB) determines whether the input is differential (1) or single-ended (0). There are 16 singled-ended channels, but only 8 differential channels. This bit should always be set to '0' if the selected internal channel is connected to an expansion card because the expansion channels are always single-ended. Bit 15 (MSB) is not used by the DAQP card and should be set to '0'.

7.2.3 Analog Input Offset Correction

The input to the A/D converter is shorted to ground if bit 14 (MSB) is set to '1' while the internal channel selection bits 8-11 specifies an internal channel of 8 or above. This can be used for analog input offset correction.

7.3 Control Register (base + 2, write)

The control register specifies the pacer clock source and pre-scaler, expansion mode, interrupt enable control and trigger control. Table 7-9 lists the control register bit definition.

Bit	Function	Explanation
7-6	Pacer clock source and pre-scaler	00 : External clock 01 : Internal, 5 MHz 10 : Internal, 1 MHz 11 : Internal, 100 kHz
5	Expansion mode	0 / 1 : disable / enable
4	EOS interrupt	0 / 1 : disable / enable
3	FIFO interrupt	0 / 1 : disable / enable
2	Trigger mode	0 / 1 : one-shot / continuous
1	Trigger source	0 / 1 : internal / external
0	Trigger edge	0 / 1 : rising / falling

Table 7-9. Control Register Bit Definition

7.3.1 Clock Source

If selected, the external clock source must not exceed 5 MHz with a minimum pulse width of 200 ns. The external clock frequency can be as low as necessary or even a DC signal and there is no limit on maximum pulse width.

7.3.2 Expansion Mode

Bit 5 must be set to '1' if there is an expansion card(s) connected to the DAQP card. All of the digital output lines (bits 0-3) will be used for external channel selection and two of the four digital input lines (bit 1 and 3) will be used for external gain selection.

7.3.3 Interrupt Enable

Bits 4 and 3 are used for interrupt enable control. The end-of-scan (EOS) interrupt will be enabled (disabled) by setting bit 4 to '1' ('0'). Setting bit 3 to '1' ('0') will enable (disable) the data FIFO interrupt when the A / D data available in the FIFO passes the almost full threshold. Since the EOS and FIFO threshold events are latched into the status register, temporarily disabling and then re-enabling the interrupt will not cause an interrupt to be lost as long as there are no repeated events during the time the interrupt is disabled.

7.3.4 Trigger Mode/Source

Bit 2 determines the trigger mode and is set to '0' for one-shot mode and '1' for continuous trigger mode.

Bit 1 specifies the trigger source and is set to '1' for external trigger (TTL trigger) and '0' for internal trigger (software trigger). When set to internal trigger, the trigger edge selection can be ignored. The external trigger signal shares the same pin on the interface connector with digital input bit 0.

7.3.5 Trigger Edge

Bit 0 selects the external trigger edge. To chose the falling edge of the external trigger signal, set this bit to '1', otherwise the rising edge is selected. Edge selection is ignored if the internal trigger source is specified.

7.4 Status Register (base + 2, read)

The status register is read only and shares the same offset as the control register. It reports data FIFO flag, interrupt and A/D conversion status. Table 7-10 lists the status register bit definition.

Bit	Status	Explanation
7	Scanning status	0/1 : busy / idle
6	Triggered status	0/1 : no / yes
5	Data lost event	0/1 : no / yes
4	End of scan event	0/1 : no / yes
3	FIFO threshold event	0/1 : no / yes
2	Data FIFO full	0/1 : false / true
1	Data FIFO almost full	0/1 : false / true
0	Data FIFO empty	0/1 : false / true

Table 7-10. Status Register Bit Definition

Bit 7 shows the scan status and is set to '0' when the DAQP card is scanning the input channels specified by the scan list and then '1' upon scan completion. '1' at bit 6 indicates the DAQP card has been triggered and is acquiring data (busy). '0' at bit 6 indicates the card is waiting for a trigger (idle). Bits 3, 4 and 5 are the event latches. When an event is detected, the corresponding bit is set to '1' until the host reads the status register which then clears all event bits to '0'. Bits 5, 4 and 3 are used for data lost, EOS and FIFO threshold events respectively. When the corresponding interrupt is enabled a '1' in bits 3 or 4 will cause an interrupt. Bits 0, 1 and 2 are the data FIFO flags.

7.5 Digital I/O Register

7.5.1 Digital Output

The four digital output lines share the same pins on the interface connector as the four external channel selection bits. When using an expansion card(s), bit 5 of the control register (base + 2) should be set to '1' so that the four digital output lines will be driven by the external channel selection bits from the scan FIFO. If bit 5 of the control register is set to "0"(default after reset), then the four output lines are driven by the values in bits 0 to 3 latched during the last write operation. In other words, the digital output bits are valid only when the DAQP card is NOT in expansion mode. Table 7-11 lists the digital output register bit definition.

Bits	Normal Mode	Expansion Mode
0-3	Digital output bits 0-3	Ignored, the four output lines will be driven by the external channel selection bits in the scan list FIFO
4-7	Reserved as all '0'	Ignored

Table 7-11. Digital Output Register Bit Definition

7.5.2 Digital Input

Two of the digital input lines are shared with the external trigger (bit 0) and the external clock (bit 2). The other two lines are used for external gain control in expansion mode (if bit 2 of the control register is set to '1'). The digital input lines are not latched.

Although the digital input lines are also used as external trigger, external clock and the external gain selection; the current status of these lines will always be returned when reading the port. The line status does not affect the digital output register. It's contents cannot be read back directly, even though they share the same port offset with the digital input register. Table 7-12 lists the digital input register bit definition.

Bits	Normal Mode	Expansion Mode
0	Digital input bit 0, also serve as external trigger	The same as in normal mode
1	Digital input bit 1	External gain select, low bit
2	Digital input bit 2, also serve as external clock	The same as in normal mode
3	Digital input bit 3	External gain select, high bit
4-7	All '0'	All '0'

Table 7-12. Digital Input Register Bit Definition

7.6 Pacer Clock (base + 4, + 5, + 6)

The pacer clock is actually a 24-bit auto-reload frequency divider. It contains a 24-bit divisor register, a 24-bit counter, an internal clock pre-scaler and a clock source multiplexer. Figure 7-1 shows the pacer clock block diagram.

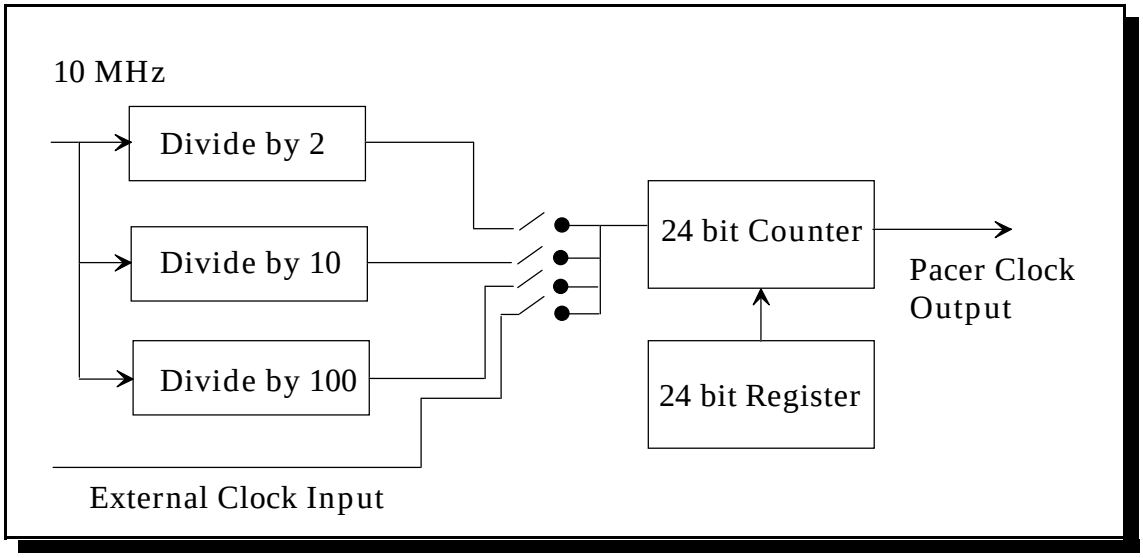

Figure 7-1. Pacer Clock Block Diagram

The clock source selection is specified by bits 6 and 7 in the control register (base + 2). The 24-bit register occupies 3 ports, in which the low byte is located at base + 3, the middle byte at base + 4 and the high byte at base + 5. All three registers are write only. The pacer clock will not generate a clock pulse output until it is triggered (either by an internal software trigger or an external TTL trigger signal in continuous mode only). In continuous mode, the trigger will serve as the first clock output pulse, and load the counter from the register. The counter will count down the input clock pulse until it is zero and then an output clock pulse is generated and the counter is reloaded. Pacer clock output will continue until the DAQP card receives the stop command which is generated by writing a '1' to bit 4 of the auxiliary control register (base + 7).

The clock rate is determined as follows: Rate = Source Frequency / (Divisor Count + 1) .

Example 1

If an internal clock source is applied at 100 kHz (control register bits 7, 6 = 11) and the divisor count is 49, then the pacer clock output frequency = 100 kHz / (49 + 1) = 2 kHz.

Example 2

If an external clock source is applied at 120 kHz (control register bits 7, 6 = 00) and the divisor count is 39, then the pacer clock output frequency = 120 kHz / (39 + 1) = 3 kHz.

7.7 Auxiliary Control Register (base + 7)

The auxiliary control register is used to send control commands to the DAQP card. It also sets the data program/access mode for the data FIFO. The command bits (bits 4 to 7) are actually "monostable" or self-cleared after the specified command function is completed. They do NOT require clearing. The data FIFO program/access bit is latched each time it is written. Table 7-13 lists the auxiliary control register bit definition.

Bit	Function	Explanation
7	Trigger/Arm command	1 = send trigger/arm, 0 = no action
6	Flush data FIFO command	1 = flush, 0 = no action
5	Flush scan list command	1 = flush, 0 = no action
4	Stop A/D command	1 = stop, 0 = no action
3	Reserved	as '0'
2-1	Scan rate selection	00 = 100, 01 = 50, 10 = 25 (kHz)
0	Data FIFO program/access	1 = data access, 0 = program threshold

Table 7-13 . Auxiliary Control Register Bit Definition

7.7.1 Trigger/Arm Command

If the trigger source is internal (software trigger), writing a '1' to bit 7 will send a trigger to the DAQP card and start the A/D conversion process. If the trigger source is external (TTL trigger), writing a '1' to bit 7 will serve as an ARM command. The ARM command tells the DAQP card to look for the specified external trigger edge from the moment the ARM command is received. Never issue the ARM command together with the A/D stop command. The ARM command initiates data acquisition and the A/D stop command terminates it.

7.7.2 Flush Scan List Queue Command

The scan list queue must be flushed before it can be programmed. This command should be issued before the flush data FIFO command. The queue may have up to 2048 word entries, each containing two bytes. It is the user's responsibility to guarantee the integrity of the entries.

7.7.3 Flush Data FIFO Command

The data FIFO should be flushed before data acquisition is initiated by the trigger/arm command, but not until after the scan list has been configured. The flush command may also be followed by FIFO threshold programming. After the FIFO is flushed, the FIFO empty flag will be set to '1' and the almost full and full flags reset to '0'. Anytime the data FIFO is flushed, the default threshold setting will be restored (7 bytes to full) by the hardware. The data FIFO threshold should always be programmed after flushing if the required threshold is different from the default one.

7.7.4 A/D Stop Command

Once data acquisition is initiated by the trigger/arm command, it can only be stopped by receiving the A/D stop command. The A/D stop command should be issued as soon as the required data points are collected to prevent data FIFO overflow. Data FIFO overflow is the only flag that indicates lost data during the acquisition process. Without the stop command, the A/D can continue to run, filling the data FIFO. When the FIFO is full, it will ignore data samples coming from the A/D converter.

7.7.5 Data FIFO Program/Access Control

The A/D data FIFO has two programmable thresholds (almost empty and almost full) and two associated flags. The almost empty threshold and flag are not used. By default, the thresholds are set to 7 bytes (7 to full and 7 to empty) when reset, powered up or anytime the FIFO is flushed. It can be programmed to any value between 1 and FIFO size - 1 (in bytes).

To program the FIFO threshold, make sure the A/D has been stopped. Set this bit to '0' by writing an all '0' byte to the auxiliary control register. Then send an A/D FIFO flush command with the same bit setting by writing a byte of 40H to the same register. This will put the FIFO into program mode. The following read/write operation will be directed to the threshold registers instead when accessing the data FIFO at base +1. The 4 byte threshold setting should be written into the data FIFO by doing four consecutive write operations. Optionally, the threshold setting can be read back for verification by doing four consecutive read operations. Table 7-14 lists the 4 byte threshold setting format.

Byte No.	Definition	Valid Range
0	Low byte of the almost empty threshold	0..255
1	High byte of the almost empty threshold	0..15
2	Low byte of the almost full threshold	0..255
3	High byte of the almost full threshold	0..15

Table 7-14. Data FIFO Threshold Setting

After the thresholds are programmed, set the access control bit to '1' by writing a byte of 01H into the auxiliary control register. This will make the following read/write operation access the data bytes in the FIFO instead of it's thresholds. It is recommended that the access control bit be set to '1' when sending other commands (flush scan list, stop A/D or trig/arm) to the DAQP card by writing into the auxiliary control register. A useful tip for safe operation is to set the bit to '0' only when flushing and programming the FIFO thresholds. Although the almost empty threshold is never used, it must be programmed because the four configuration bytes must be accessed as an entire entity.

7.7.6 Scan Rate Selection

Depending on the input mode and the gain selection, the analog front end may have different settling times. In order to give the best performance, the DAQP card allows the user to choose three different scanning rates by setting bit 2 and bit 3 while the start A/D command is issued. The default scanning rate is 100 kHz (bits 2-3 set to '00'). A scan rate of 50kHz can be selected by setting the bits to '01' and 25 kHz by setting them to '10'. Setting the bits to '11' gives the same result as '01'.

It is recommended that the scan rate setting be issued in conjunction with the trigger/arm command and kept unchanged during data acquisition. For example, writing 81H to the auxiliary control register will start data acquisition with the scan rate set to 100 kHz, (use 83H for 50 kHz and 85H for 25 kHz**).**

8. I/O Connections

The DAQP card is fitted with a 32-pin shielded connector. See Figure 8-1 for pin assignments. A mating connector and shield are available from Hirose for the D-32 output connector.

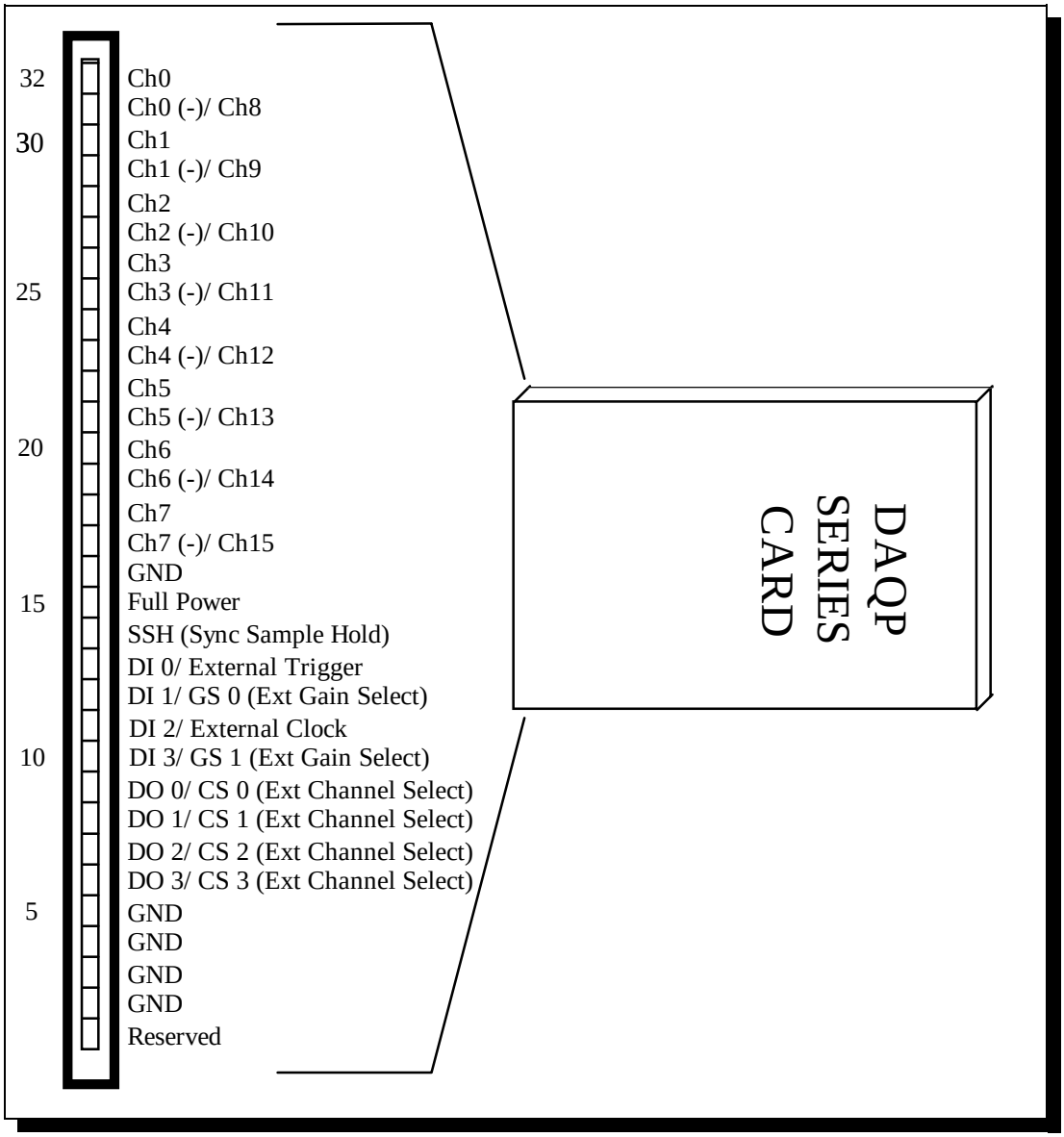

Figure 8-1. DAQP Series Card Hirose-32 Output Connector

9. Optional Accessories

9.1 UIO-37 Screw Terminal Block

For applications requiring discrete wiring connections, the UIO-37 terminal block provides a simple way of connecting signals to the DAQP card. The D37 connector is available in either male or female and has two rows of screw terminals. The first row is numbered from pin 1 to pin 19 and the second row from pin 20 to pin 37, (see Figure 9-1).

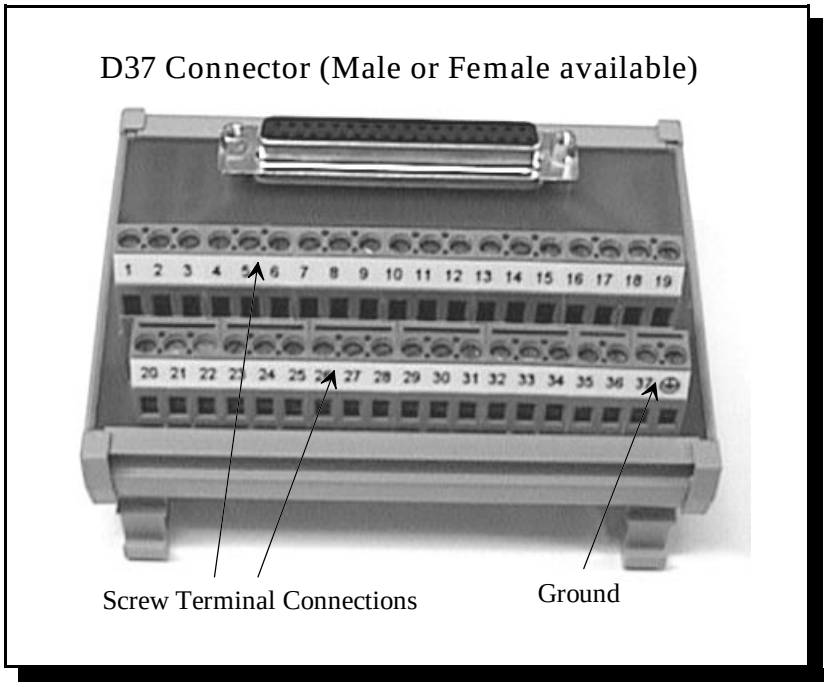

Figure 9-1. UIO-37 Terminal Block

9.2 CP-DAQP Cable Assembly

An optional cable assembly, part number CP-DAQP, is available for converting the DAQP card's Hirose 32-pin I/O connector to a standard D-37 male connector. The D-37 connector is compatible with the P-1 connector of the Keithley DAS-1600®. Figure 9-1 illustrates accessory connections.

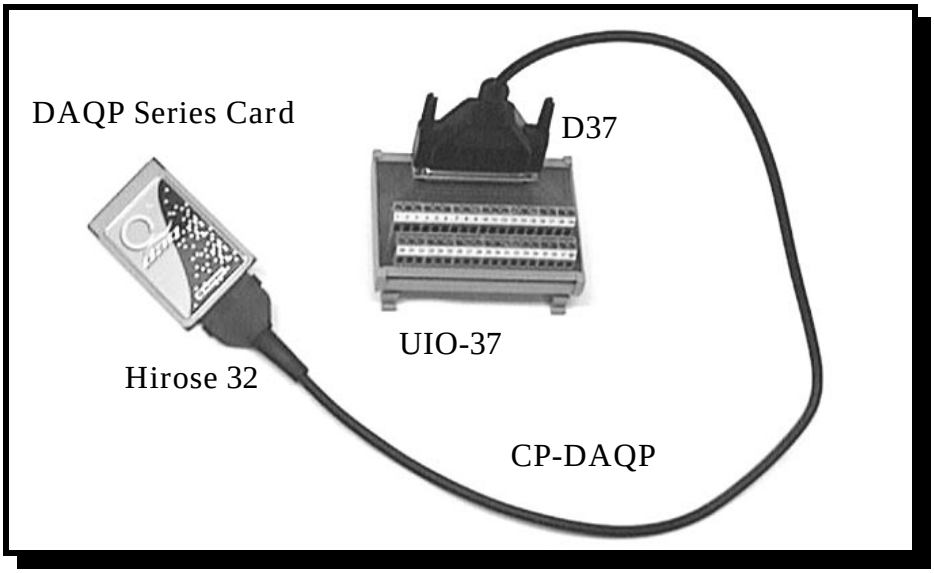

Figure 9-1. DAQP Series Card Accessory Connection

Figure 9-3 illustrates the D-37 connector pin assignments for the CP-DAQP and UIO-37.

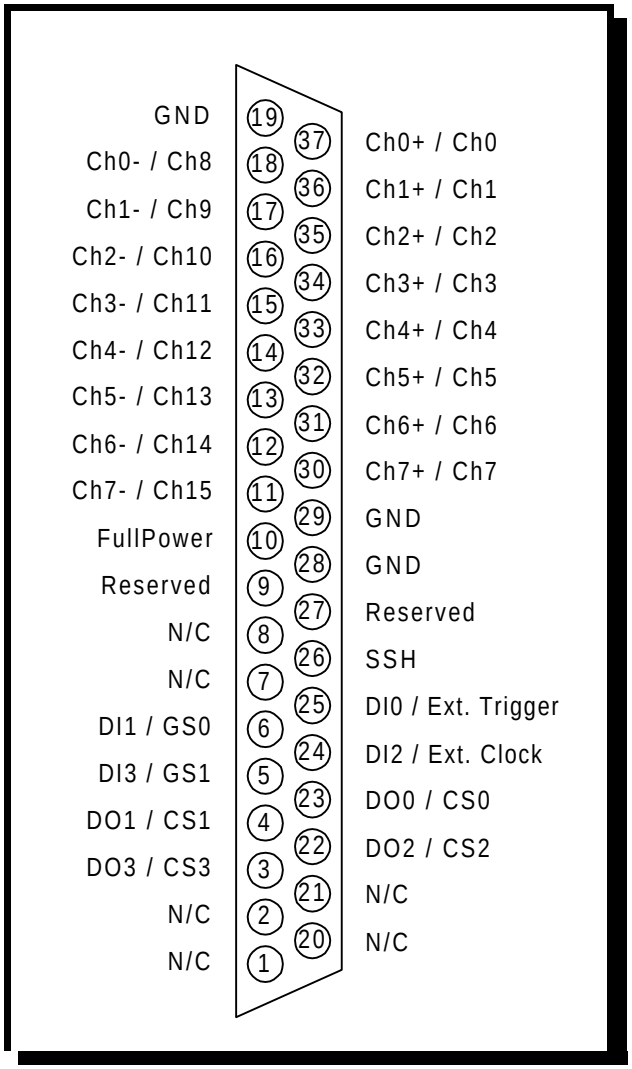

Figure 9-3. CP-DAQP / UIO-37 D-37 Pin Diagram

Table 9-1 lists cable mapping for the CP-DAQP Hirose-32 to D37 connector.

Hirose-32	D-37	Name		Description
32	37	Channel 0 (+)		Channel 0
31	18	Channel 0 (-)	Channel 8	A/D input, differential / single-ended
30	36	Channel 1 (+)	Channel 1	A/D input, differential / single-ended
29	17	Channel 1 (-)	Channel 9	A/D input, differential / single-ended
28	35	Channel 2 (+)	Channel 2	A/D input, differential / single-ended
27	16	Channel 2 (-)	Channel 10	A/D input, differential / single-ended
26	34	Channel 3 (+)	Channel 3	A/D input, differential / single-ended
25	15	Channel 3 (-)	Channel 11	A/D input, differential / single-ended
24	33	Channel 4 (+)	Channel 4	A/D input, differential / single-ended
23	14	Channel 4 (-)	Channel 12	A/D input, differential / single-ended
22	32	Channel 5 (+)	Channel 5	A/D input, differential / single-ended
21	13	Channel 5 (-)	Channel 13	A/D input, differential / single-ended
20	31	Channel 6 (+)	Channel 6	A/D input, differential / single-ended
19	12	Channel 6 (-)	Channel 14	A/D input, differential / single-ended
18	30	Channel 7 (+)	Channel 7	A/D input, differential / single-ended
17	11	Channel 7 (-)	Channel 15	A/D input, differential / single-ended
16	29	GND		A/D input, differential / single-ended
15	10	FullPower (org. D/A 0 ref. in)		1/0 : Full power / Power down
14	26	SSH (org. D/A 1 ref. in)		Synchronous Sample Hold
13	25	Digital in bit 0 (shared)		External trigger (same as in DAS-16)
12	6	Digital in bit 1 (normal mode)		External gain, LSB (expansion mode)
11	24	Digital in bit 2 (shared)		External clock (org. DAS-16 Ctr 0 Gate)
10	5	Digital in bit 3 (normal mode)		External gain, MSB (expansion mode)
9	23	Digital out bit 0 (normal		External channel bit 0 (expansion mode)
8	4	Digital out bit 1 (normal		External channel bit 1 (expansion mode)
7	22	Digital out bit 2 (normal		External channel bit 2 (expansion mode)
6	3	Digital out bit 3 (normal		External channel bit 3 (expansion mode)
5	28	GND		
4	28	GND		
3	19	GND		
2	19	GND		
1	27	Reserved		D/A output channel 1

Table 9-1. DAQP Series Card Cable Mapping

10. Specifications

A/D Converter	**12-Bit Version**	**16-Bit Version**
Acquisition + Conversion	2 ms + 8 ms	2 ms + 8 ms
Monotonicity	No missing codes	No missing codes
Integral linearity error	± 1 LSB	± 3 LSB
Differential linearity error	± 1 LSB	+3/-2 LSB
Full scale error	± 0.5 %	± 0.5 %
Aperture delay	40 ns	40 ns

Analog Input		
Number of input channels	8 differential / 16 single-ended, expandable to 256	
Input range	±10, ±5, ±2.5, ±1.25V	(DAQP-12/DAQP-16)
	±10, ±1, ±0.1, ±0.01V	(DAQP-12H)
Programmable gain	1, 2, 4, 8	(DAQP-12/DAQP-16)
	1, 10, 100, 1000	(DAQP-12H)
Maximum over-voltage	±30 V	
Input impedance	100 MW (DC)	

A/D Miscellaneous Specifications	
Data FIFO depth	2048 samples
Scan list length	2048 entries
Scan speed	10 ms, 20 ms, 40 ms
Trigger source	Internal (Software) / External (TTL)
Trigger mode	Continuous / One-shot
External (TTL) trigger	0.8 V (low) / 2.2 V (high), Rising / Falling edges
	Latency to A/D scan < 1 ms
Sampling rate	0.006 Hz to 100 kHz (with internal clock source)
External clock rate	DC - 5 MHz

Digital I/O	
Digital input channels	4 (no latch)
Digital output channels	4 (latched)
Maximum source current	0.5 mA
Maximum sinking current	2.5 mA
Minimum logic ‘1’ level	2.4 V
Maximum logic ‘0’ level	0.8 V

General Specifications	
Power consumption	160 mA (full power), 40 mA (power down)
Operating temperature	0 °C to 50 °C
Storage temperature	0 °C to 70 °C
Humidity	0 to 95%, non-condensing
Size (cable not included)	Standard PCMCIA type II
Weight	1.5 oz (for reference only)

DAQP-12/12H/16 PCMCIA
Data Acquisition System Users Manual
Version 2.40
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